CLAIMS

WHAT IS CLAIMED:

1. A method comprising:

forming a process layer above a semiconducting substrate;

etching at least a portion of said process layer;

measuring a first depth of the etch at a first location in a first preselected region of the semiconducting substrate;

comparing the first depth to a desired depth; and

varying the temperature of a subsequently processed semiconducting substrate in a region corresponding to the first preselected region in response to the first depth being different from the desired depth.

2. A method, as set forth in claim 1, further comprises:

measuring the depth of the etch at a second location in a second preselected region of the semiconducting substrate;

comparing the second depth to a desired depth; and

varying the temperature of the subsequently processed semiconducting substrate in a region corresponding to the second preselected region in response to the second depth being different from the desired depth.

3. A method, as set forth in claim 1, wherein comparing the first depth to a desired depth further comprises:

measuring a second depth of the etch at a second location in a second preselected region of the semiconducting substrate; and

setting the desired depth to the second depth.

4. A method, as set forth in claim 2, wherein varying the temperature further comprises raising the temperature of the subsequently processed semiconducting substrate in the region corresponding to the second preselected region in response to the second depth being less than the desired depth.

5. A method, as set forth in claim 2, wherein varying the temperature further comprises lowering the temperature of the subsequently processed semiconducting substrate in the region corresponding to the second preselected region in response to the second depth being greater than the desired depth.

6. A method, as set forth in claim 1, wherein forming a process layer above a semiconducting substrate comprises forming a process layer comprised of at least one of an oxide, an oxynitride, polysilicon, and a metal above a semiconducting substrate.

7. A method, as set forth in claim 1, wherein etching at least a portion of said process layer further comprises performing a plasma etching process on at least a portion of the process layer.

8. A method, as set forth in claim 1, wherein varying the temperature of the subsequently processed semiconducting substrate in the region corresponding to the first preselected region further comprises varying the temperature of the subsequently processed

semiconducting substrate in the region corresponding to the first preselected region as a function of the difference.

9. A method, as set forth in claim 1, wherein measuring the first depth further comprises:

measuring the depth at a plurality of locations in the first region; and

averaging the plurality of measured depths to determine the first depth.

10. A method, as set forth in claim 1, wherein measuring the first depth further comprises:

measuring the depth at a plurality of locations in the first region; and

selecting the smallest measured depth to be the first depth.

11. A method, as set forth in claim 1, wherein measuring the first depth further comprises:

measuring the depth at a plurality of locations in the first region; and

selecting the greatest measured depth to be the first depth.

12. A method, as set forth in claim 1, wherein measuring the first depth further comprises:

measuring the depth at a plurality of locations in the first region; and

selecting the median measured depth to be the first depth.

13. A method comprising:

forming a process layer above a semiconducting substrate;

etching at least a portion of said process layer;

measuring a first depth of the etch at a first location in a first preselected region of the semiconducting substrate;

measuring a second depth of the etch at a second location in a second preselected region of the semiconducting substrate;

comparing the first depth to a desired depth;

varying the temperature of a subsequently processed semiconducting substrate in a region corresponding to the first preselected region in response to the first depth being different from the desired depth;

comparing the second depth to a desired depth; and

varying the temperature of a subsequently processed semiconducting substrate in a region corresponding to the second preselected region in response to the second depth being different from the desired depth.

14. A method, as set forth in claim 13, wherein varying the temperature further comprises raising the temperature of the subsequently processed semiconducting substrate in the region corresponding to the second preselected region in response to the second depth being less than the desired depth.

15. A method, as set forth in claim 13, wherein varying the temperature further comprises raising the temperature of the subsequently processed semiconducting substrate in the region corresponding to the first preselected region in response to the first depth being less than the desired depth.

16. A method, as set forth in claim 13, wherein forming a process layer above a semiconducting substrate comprises forming a process layer comprised of at least one of an oxide, an oxynitride, polysilicon, and a metal above a semiconducting substrate.

17. A method, as set forth in claim 13, wherein etching at least a portion of said process layer further comprises performing a plasma etching process on at least a portion of the process layer.

18. A method, as set forth in claim 13, wherein varying the temperature of the subsequently processed semiconducting substrate in the region corresponding to the first preselected region further comprises varying the temperature of the subsequently processed semiconducting substrate in the region corresponding to the first preselected region as a function of the difference.

19. A method, as set forth in claim 13, wherein measuring the first depth further comprises:

measuring the depth at a plurality of locations in the first region; and

averaging the plurality of measured depths to determine the first depth.

20. A method, as set forth in claim 13, wherein measuring the first depth further comprises:

measuring the depth at a plurality of locations in the first region; and

selecting the smallest measured depth to be the first depth.

21. A method, as set forth in claim 13, wherein measuring the first depth further comprises:

measuring the depth at a plurality of locations in the first region; and

selecting the greatest measured depth to be the first depth.

22. A method, as set forth in claim 13, wherein measuring the first depth further comprises:

measuring the depth at a plurality of locations in the first region; and

selecting the median measured depth to be the first depth.

23. A method comprising:

forming a process layer above a semiconducting substrate;

etching at least a portion of said process layer;

measuring a first depth of the etch at a first location in a first preselected region of the semiconducting substrate;

measuring a second depth of the etch at a second location in a second preselected region of the semiconducting substrate;

comparing the first depth to the second depth;

varying the temperature of a subsequently processed semiconducting substrate in a region corresponding to the first preselected region in response to the first depth being different from the second depth.

24. A method, as set forth in claim 23, wherein varying the temperature further comprises raising the temperature of the subsequently processed semiconducting substrate in

the region corresponding to the first preselected region in response to the first depth being less than the second depth.

25. A method, as set forth in claim 23, wherein varying the temperature further comprises lowering the temperature of the subsequently processed semiconducting substrate in the region corresponding to the first preselected region in response to the first depth being greater than the second depth.

26. A method, as set forth in claim 23, wherein forming a process layer above a semiconducting substrate comprises forming a process layer comprised of at least one of an oxide, an oxynitride, polysilicon, and a metal above a semiconducting substrate.

27. A method, as set forth in claim 23, wherein etching at least a portion of said process layer further comprises performing a plasma etching process on at least a portion of the process layer.

28. A method, as set forth in claim 23, wherein varying the temperature of the subsequently processed semiconducting substrate in the region corresponding to the first preselected region further comprises varying the temperature of the subsequently processed semiconducting substrate in the region corresponding to the first preselected region as a function of the difference.

29. A method, as set forth in claim 23, wherein measuring the first depth further comprises:

measuring the depth at a plurality of locations in the first region; and

averaging the plurality of measured depths to determine the first depth.

30. A method, as set forth in claim 23, wherein measuring the first depth further comprises:

measuring the depth at a plurality of locations in the first region; and

selecting the smallest measured depth to be the first depth.

31. A method, as set forth in claim 23, wherein measuring the first depth further comprises:

measuring the depth at a plurality of locations in the first region; and

selecting the greatest measured depth to be the first depth.

32. A method, as set forth in claim 23, wherein measuring the first depth further comprises:

measuring the depth at a plurality of locations in the first region; and

selecting the median measured depth to be the first depth.

33. A system, comprising:

a semiconductor processing tool capable of forming a process layer above a semiconducting substrate;

an etcher capable of removing at least a portion of the process layer;

a metrology tool capable of measuring a first depth of the etch at a first location in a first preselected region of the semiconducting substrate;

a controller capable of comparing the first depth to a desired depth, and varying the temperature of a subsequently processed semiconducting substrate in a region corresponding

to the first preselected region in response to the first depth being different from the desired depth.

34. A system, as set forth in claim 33, wherein the metrology tool is capable of measuring a second depth of the etch at a second location in a second preselected region of the semiconducting substrate, and the controller is capable of setting the second depth to the desired depth.

35. A system, as set forth in claim 33, further comprising:

the metrology tool being capable of measuring the depth of the etch at a second location in a second preselected region of the semiconducting substrate; and

the controller being capable of comparing the second depth to a desired depth, and varying the temperature of the subsequently processed semiconducting substrate in a region corresponding to the second preselected region in response to the second depth being different from the desired depth